DESCRIPTION

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device of a double diffused MOS structure employing a silicon carbide semiconductor substrate, and a manufacturing method for the semiconductor device.

BACKGROUND ART

[0002] In a double diffused MOS (DMOS) FET employing a silicon carbide (SiC) semiconductor substrate, an n^--type SiC semiconductor epitaxial layer is provided on a surface of an n^+-type SiC semiconductor substrate. A p-type impurity region is provided in a surface portion of the n^--type SiC semiconductor epitaxial layer, and an n^+-type impurity region having an annular shape as seen in plan is provided in the p-type impurity region.

[0003] Fig. 7 is a diagram illustrating an impurity profile in the p-type impurity region in the prior-art double diffused MOSFET. In the prior-art double diffused MOSFET, the p-type impurity region has a so-called box profile. That is, the profile in the p-type impurity region in the prior-art double diffused MOSFET is

controlled as having a generally uniform impurity concentration irrespective of the depth from the surface of the p-type impurity region.

[0004] The p-type impurity region having such a box profile is formed by implanting a p-type impurity into the surface portion of the n^--type SiC semiconductor epitaxial layer by multi-step ion implantation. Ion implantation performed with constant implantation energy (single-step ion implantation) provides a depthwise impurity distribution approximate to the Gaussian distribution (as indicated by two-dot-and-dash lines in Fig. 7). Therefore, by performing ion implantation with three different levels of implantation energy (three-step ion implantation), for example, a near surface of the p-type impurity region and the deepest portion of the p-type impurity region (on a boundary between the p-type impurity region and the n^--type SiC semiconductor epitaxial layer) are allowed to have substantially the same impurity concentration.

[0005] When the deep portion of the p-type impurity region has a lower impurity concentration, a depletion layer is liable to spread into the p-type impurity region from the boundary between the p-type impurity region and the n^--type SiC semiconductor epitaxial layer, so that punch-through is liable to occur. Therefore, a breakdown

voltage of the prior-art double diffused MOSFET is sufficiently increased by setting the impurity concentration of the p-type impurity region at a high level on the order of 10^{17} to $10^{18}/cm^3$. However, where the p-type impurity region has a high impurity concentration, carriers moving in a channel region are liable to be scattered. This disadvantageously reduces the carrier mobility in the channel (increases the ON resistance).

DISCLOSURE OF THE INVENTION

[0006] It is therefore an object of the present invention to provide a semiconductor device having a structure which ensures both a higher breakdown voltage for suppression of punch-through and an improved carrier mobility in a channel at the same time, and to provide a manufacturing method of the semiconductor device.

[0007] A semiconductor device according to the present invention is a semiconductor device of a double diffused MOS structure employing a silicon carbide semiconductor substrate. The semiconductor device comprises a silicon carbide semiconductor epitaxial layer provided on a surface of the silicon carbide semiconductor substrate and having a first conductivity which is the same conductivity as the silicon carbide semiconductor substrate, and an impurity region formed by doping a surface

portion of the silicon carbide semiconductor epitaxial layer with an impurity of a second conductivity, the impurity region having a profile such that a near surface thereof has a relatively low second-conductivity impurity concentration and a deep portion thereof has a relatively high second-conductivity impurity concentration.

[0008] With this arrangement, the deep portion of the impurity region has a higher second-conductivity impurity concentration, so that a depletion layer is prevented from spreading into the impurity region from a boundary between the impurity region and the underlying silicon carbide semiconductor epitaxial layer. On the other hand, the near surface of the impurity concentration, so that carriers moving in a channel region formed in a surface portion of the impurity region are less liable to be scattered. Thus, the mobility of the carriers in the channel can be kept high. This makes it possible to ensure both a high breakdown voltage for suppression of punch-through and an improved carrier mobility in the channel at the same time.

[0009] The profile of the impurity region is preferably such that a near deepest portion of the impurity region (adjacent to the boundary between the impurity region and the silicon carbide semiconductor epitaxial layer) has a high peak second-conductivity impurity concentration

on the order of not lower than $10^{18}/cm^3$ and the second-conductivity impurity concentration continuously and gently decreases from the peak concentration level in the near deepest portion toward the near surface of the impurity region in which the second-conductivity impurity concentration is not higher than $5\times10^{15}/cm^3$.

[0010] A second-conductivity impurity concentration in an outermost surface portion of the impurity region is preferably controlled to be lower than a first-conductivity impurity concentration in the silicon carbide semiconductor epitaxial layer. Thus, the second-conductivity impurity concentration in the outermost surface portion of the impurity region is lower than the first-conductivity impurity concentration in the silicon carbide semiconductor epitaxial layer, so that an accumulation MOSFET structure can be provided in which a first conductivity appears in the surface portion (channel region) of the impurity region and the channel region of the first conductivity serves as an accumulation layer. Therefore, a threshold voltage is reduced, and the carrier mobility in the channel is further improved.

[0011] A semiconductor device manufacturing method according to the present invention is a method for manufacturing a semiconductor device of a double diffused MOS structure employing a silicon carbide semiconductor

substrate. The method comprises steps of: forming a silicon carbide semiconductor epitaxial layer having a first conductivity on a surface of the silicon carbide semiconductor substrate, the first conductivity being the same conductivity as the silicon carbide semiconductor substrate; and doping a surface portion of the silicon carbide semiconductor epitaxial layer with an impurity of a second conductivity to form an impurity region having a profile such that a near surface thereof has a relatively low second-conductivity impurity concentration and a deep portion thereof has a relatively high second-conductivity impurity concentration.

[0012] The semiconductor device described above can be manufactured by this method.

[0013] The impurity region having the profile with the second-conductivity impurity concentration being relatively low in the near surface thereof and relatively high in the deep portion thereof can be formed by doping the surface portion of the silicon carbide semiconductor epitaxial layer with the impurity of the second conductivity by single-step ion implantation.

[0014] In the impurity region forming step, the impurity region is preferably formed as having a profile such that a second-conductivity impurity concentration in an outermost surface portion thereof is lower than a

first-conductivity impurity concentration in the silicon carbide semiconductor epitaxial layer. Thus, the semiconductor device can be manufactured in which the second-conductivity impurity concentration in the outermost surface portion of the impurity region is controlled to be lower than the first-conductivity impurity concentration in the silicon carbide semiconductor epitaxial layer.

[0015] The foregoing and other objects, features and effects of the present invention will become more apparent from the following description of embodiments with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view schematically illustrating a construction of a semiconductor device according to an embodiment of the present invention;

Fig. 2 is a diagram illustrating an impurity profile of a p-type impurity region of the semiconductor device;

Fig. 3 is a sectional view schematically illustrating a construction of an accumulation MOSFET;

Fig. 4 is a sectional view schematically illustrating a construction of a semiconductor device according to another embodiment of the present invention;

Fig. 5 is a diagram illustrating an impurity profile

of a p-type impurity region of the semiconductor device shown in Fig. 4;

Fig. 6 is a graph illustrating gate characteristics of the semiconductor device shown in Fig. 4; and

Fig. 7 is a diagram illustrating an impurity profile of a p-type impurity region of a prior-art double diffused MOSFET.

BEST MODE FOR IMPLEMENTING THE INVENTION

[0016] Fig. 1 is a sectional view schematically illustrating a construction of a semiconductor device according to an embodiment of the present invention. The semiconductor device is a double diffused MOSFET, and employs an n^+-type SiC semiconductor substrate 1 as a semiconductor substrate.

[0017] An n^--type SiC semiconductor epitaxial layer 2 having a lower impurity concentration than the n^+-type SiC semiconductor substrate 1 is provided on a surface of the n^+-type SiC semiconductor substrate 1. A p-type impurity region 3 having a rectangular shape as seen in plan, for example, is provided in a surface portion of the n^--type SiC semiconductor epitaxial layer 2. Further, an n^+-type impurity region 4 having a rectangular frame shape as seen in plan is provided in the p-type impurity region 3 in properly spaced relation from peripheral edges

of the p-type impurity region 3. The p-type impurity region 3 has a depth of 0.5 to 0.7μm from a surface of the n^--type SiC semiconductor epitaxial layer 2. The n^+-type impurity region 4 has a depth of 0.2 to 0.3μm from the surface of the n^--type SiC semiconductor epitaxial layer 2. A portion of the p-type impurity region 3 present below the n^+-type impurity region 4 has a thickness of at least 0.2 to 0.3μm.

[0018] Gate oxide films 5a, 5b and gate electrodes 6a, 6b are provided on the n^--type SiC semiconductor epitaxial layer 2. The gate oxide films 5a, 5b are each linearly provided along one of the peripheral edges of the p-type impurity region 3 (n^+-type impurity region 4) as spanning an area between an outer peripheral portion of the n^+-type impurity region 4 and the outside of the p-type impurity region 3. The gate oxide films 5a, 5b each cover a portion of the surface of the n^--type SiC semiconductor epitaxial layer 2 between the outer peripheral edge portion of the n^+-type impurity region 4 and the outside of the p-type impurity region 3. The gate electrodes 6a, 6b are respectively provided on the gate oxide films 5a, 5b.

[0019] An inter-layer insulation film 7 is provided over the gate electrodes 6a, 6b. A source electrode 8 having, for example, a rectangular shape as seen in plan is provided over the inter-layer insulation film 7. The

source electrode 8 is connected to a source contact region including an inner peripheral portion of the n^+-type impurity region 4 and a region of the p-type impurity region 3 surrounded by the n^+-type impurity region 4 via a contact hole 71 formed in the inter-layer insulation film 7.

[0020] A drain electrode 9 is provided on a rear side of the n^+-type SiC semiconductor substrate 1 (opposite from the n^--type SiC semiconductor epitaxial layer 2) as covering the entire rear surface.

[0021] Fig. 2 is a diagram illustrating an impurity profile of the p-type impurity region 3. The p-type impurity region 3 is formed by forming the n^--type SiC semiconductor epitaxial layer 2 on the surface of the n^+-type SiC semiconductor substrate 1 by epitaxial growth and then implanting, for example, aluminum (Al) ions as the p-type impurity into the surface portion of the n^--type SiC semiconductor epitaxial layer 2 with an implantation energy of 400keV (constant). That is, the formation of the p-type impurity region 3 is achieved by single-step ion implantation with an implantation energy of 400keV.

[0022] The p-type impurity region 3 thus formed has an impurity profile such that a near deepest portion thereof (adjacent to a boundary between the p-type impurity region and the n^--type SiC semiconductor epitaxial layer 2) present at a depth of 0.5 to 0.7μm has a high peak p-type

impurity concentration on the order of not lower than $10^{18}/cm^3$ and the p-type impurity concentration continuously and gently decreases from the peak concentration level in the near deepest portion toward a near surface in which the p-type impurity concentration is not higher than $5\times10^{15}/cm^3$, because the impurity introduced into the n^--type SiC semiconductor epitaxial layer 2 partly collides on SiC crystals to be reflected back.

[0023] Since the impurity concentration is high in a deep portion of the p-type impurity region 3, a depletion layer is prevented from spreading into the p-type impurity region 3 from the boundary between the p-type impurity region 3 and the underlying n^--type SiC semiconductor epitaxial layer 2. On the other hand, the impurity concentration is low in the near surface of the p-type impurity region 3, so that carriers moving in a channel region formed in a surface portion of the p-type impurity region 3 are less liable to be scattered. Thus, mobility of the carriers in the channel can be kept high. Therefore, the double diffused MOSFET structure ensures both a high breakdown voltage for suppression of punch-through and an improved carrier mobility in the channel at the same time.

[0024] Where a p-type impurity concentration in an outermost surface portion of the p-type impurity region

3 is lower than the n-type impurity concentration of the n^--type SiC semiconductor epitaxial layer 2 (e.g., $10^{16}/cm^3$), an accumulation MOSFET structure can be provided in which an n^--type conductivity appears, as shown in Fig. 3, in the surface portion (channel region) of the p-type impurity region 3 and the n^--type channel region serves as an accumulation layer 31. Therefore, the carrier mobility in the channel is further improved.

[0025] Fig. 4 is a sectional view schematically illustrating the construction of a semiconductor device according to another embodiment of the present invention. The semiconductor device is an accumulation MOSFET, and employs an n^+-type SiC semiconductor substrate 11 as a semiconductor substrate.

[0026] An n^--type SiC semiconductor epitaxial layer 12 having a lower impurity concentration than the n^+-type SiC semiconductor substrate 11 is provided on a surface of the n^+-type SiC semiconductor substrate 11. A p-type impurity region 13 is provided in a surface portion of the n^--type SiC semiconductor epitaxial layer 12. Further, an n^+-type source region 14 and an n^+-type drain region 15 are provided in a surface portion of the p-type impurity region 13 in properly spaced relation from each other. An n-type accumulation layer 16 is provided in a channel region between the n^+-type source region 14 and the n^+-type

drain region 15.

[0027] The p-type impurity region 13 has a depth of 0.5 to 0.7μm from a surface of the n^--type SiC semiconductor epitaxial layer 12. The n^+-type source region 14 and the n^+-type drain region 15 each have a depth of 0.2 to 0.3μm from the surface of the n^--type SiC semiconductor epitaxial layer 12. The n-type accumulation layer 16 has a depth of 0.05 to 0.1μm from the surface of the n^--type SiC semiconductor epitaxial layer 12.

[0028] A source electrode 17 and a drain electrode 18 are respectively provided on the n^+-type source region 14 and the n^+-type drain region 15. A gate oxide film 19 is provided on a portion of the n^--type SiC semiconductor epitaxial layer 12 between the source electrode 17 and the drain electrode 18, and a gate electrode 20 is provided on the gate oxide film 19.

[0029] Fig. 5 is a diagram illustrating an impurity profile of the p-type impurity region 13. The p-type impurity region 13 is formed by forming the n^--type SiC semiconductor epitaxial layer 12 on the surface of the n^+-type SiC semiconductor substrate 11 by epitaxial growth and then implanting, for example, aluminum (Al) ions as the p-type impurity into the surface portion of the n^--type SiC semiconductor epitaxial layer 12 with an implantation energy of 400keV (constant). That is, the formation of

the p-type impurity region 13 is achieved by single-step ion implantation with an implantation energy of 400keV.

[0030] Where the p-type impurity region 13 is thus formed as having a depth of about 0.7μm (7000Å) from the surface of the n^--type SiC semiconductor epitaxial layer 12, the p-type impurity region 13 has an impurity profile such that a near deepest portion thereof (adjacent to a boundary between the p-type impurity region and the n^--type SiC semiconductor epitaxial layer 12) has a high peak p-type impurity concentration (atom density) on the order of not lower than $10^{18}/cm^3$ and the p-type impurity concentration continuously and gently decreases from the peak concentration level in the near deepest portion toward a surface, because the impurity introduced into the n^--type SiC semiconductor epitaxial layer 12 partly collides on SiC crystals to be reflected back. The p-type impurity concentration in a near surface is not higher than one hundredth the peak p-type impurity concentration, more specifically not higher than $5\times10^{15}/cm^3$. In the impurity profile, the p-type impurity concentration changes steeply in a portion deeper than the near deepest portion having the peak impurity concentration and changes much more gently in a portion between the near deepest portion and the surface than in the portion deeper than the near deepest portion.

[0031] Since the n-type impurity concentration (atom density) in the n^--type SiC semiconductor epitaxial layer 12 is generally constant on the order of $10^{16}/cm^3$, the p-type impurity concentration in the surface portion (channel region) of the p-type impurity region 13 is lower than the n-type impurity concentration. As a result, an n-type conductivity appears in the surface portion of the p-type impurity region 13 to form the n-type accumulation layer 16.

[0032] As shown in Fig. 6, the accumulation MOSFET with its n-type accumulation layer 16 thus formed has more excellent characteristics than a prior-art MOSFET having a p-type impurity region formed as having substantially the same depth as the p-type impurity region 13 in a surface portion of an n^--type SiC semiconductor epitaxial layer by performing ion implantation with four different levels of implantation energy (four-step ion implantation).

[0033] That is, the prior-art MOSFET has a threshold voltage of about 8.0V and a carrier mobility of about $18.3cm^2/Vs$ in the channel. Where a gate voltage is 15V, a drain current is about 19μA. In contrast, the accumulation MOSFET has a reduced threshold voltage on the order of 3.3V. In addition, the threshold voltage is positive, so that the accumulation MOSFET is of a normally OFF type which is required for a power switching element.

Further, carrier mobility in a channel is improved to about $24cm^2/Vs$. In addition, a drain current is about 42μm where a drain voltage is 15V, so that an ON resistance is reduced to one half as compared with the prior-art MOSFET.

[0034] A formation of a buried channel such as the n-type accumulation layer 16 may be achieved by forming an n-type layer by epitaxial growth after the formation of the p-type impurity region (e.g., Japanese Unexamined Patent Publication No. 10-308510). Alternatively, the formation may be achieved by performing multi-step ion implantation to selectively implant the n-type impurity into the p-type impurity region after the formation of the p-type impurity region (e.g., Japanese Unexamined Patent Publication No. 11-261061).

[0035] Where the buried channel is formed by the epitaxial growth, the epitaxial growth should be stopped at an initial stage to provide a thin n-type layer having a depth of about 0.1 to 0.2μm. However, it is difficult to precisely control an impurity concentration and a depth at the initial stage of the epitaxial growth. Therefore, it is impossible to control the impurity concentration and the depth of the buried channel as designed, which presents a problem that an accumulation MOSFET is liable to be of a normally ON type.

[0036] In the ion implantation, it is possible to

precisely control the depth of the buried channel. However, the n-type impurity is implanted with a high concentration to cancel the p-type conductivity of the p-type impurity region, so that the buried channel has a high impurity concentration. This results in a problem that the impurity concentration of the buried channel cannot be controlled as designed, because a rate of impurity activation by annealing after the ion implantation is unstable. The buried channel having a high impurity concentration also suffers from a problem that carriers are susceptible to coulomb scattering and, hence, carrier mobility in the channel is lower.

[0037] In contrast, the method according to this embodiment (involving the formation of the n-type accumulation layer 16) is free from the problem encountered where the buried channel is formed by the epitaxial growth. Further, the n-type accumulation layer 16 has a low impurity concentration, so that the accumulation MOSFET is manufactured as having a normally OFF characteristic as designed without an influence of a rate of the activation by the annealing. Further, the n-type accumulation layer 16 has a high carrier mobility with a smaller degree of coulomb scattering of the carriers.

[0038] While the two embodiments of the present invention have thus been described, the invention may be

embodied in other ways. In the embodiments described above, the n-type SiC semiconductor substrate is employed by way of example, but the semiconductor device having the double diffused MOS structure can be manufactured in substantially the same manner even, for example, by employing a p-type SiC semiconductor substrate. It is also possible to manufacture a semiconductor device of a CMOS structure.

[0039] While the present invention has been described in detail by way of the embodiments thereof, it should be understood that these embodiments are merely illustrative of the technical principles of the present invention but not limitative of the invention. The spirit and scope of the present invention are to be limited only by the appended claims.

[0040] This application corresponds to Japanese Patent Application No. 2004-54506 filed with the Japanese Patent Office on February 27, 2004, the disclosure of which is incorporated herein by reference.